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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR   | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|------------------------|---------------------|------------------|
| 09/866,357      | 05/25/2001  | Ronald DeShawn Blanton | 5347-210            | 5572             |

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PO BOX 37428  
RALEIGH, NC 27627

EXAMINER

IQBAL, NADEEM

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2114

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/866,357

Applicant(s)

BLANTON

Examiner

Nadeem Iqbal

Art Unit

2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 May 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-55 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 52-55 is/are allowed.
- 6) ☒ Claim(s) 1,10,17,24,31,38 and 45 is/are rejected.
- 7) ☐ Claim(s) 2-9,11-16,18-23,25-30,32-37,39-44 and 46-51 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith

(Article, Model for delay faults based upon paths, 1985 International test conference, an IDS provided by the Applicant).

3. Smith teaches (Page 342, Intro. Lines 1-10) testing of a clocked machine for delay

failures that includes that after initial loading of the latches feeding the network, a clock is issued that causes many of these latches to take on new values, the clock that samples the output of the network into another set of latches is timed to occur at the same time interval. He thus teaches defining a fault tuple including identification of a signal line, a signal value, and a clock cycle constraint for the signal line. He does not explicitly disclose a test sequence that comprises one of more test patterns where the signal line is controlled to the signal line value during a clock cycle of the test sequence. He teaches as stated above that the clock that samples the output of the network another set of latches is timed to occur at the same time interval after the previous clock as occurs during normal machine operation. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that he teaches a signal line that is controlled to the signal line value during a clock cycle of the test sequence, since he

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teaches a clock that samples the output of the network into another set of latches is timed to occur at the same time interval as the previous clock.

*Allowable Subject Matter*

4. Claims 52-55 are allowed.
5. Claims 2-9, 11-16, 18-23, 25-30, 32-37, 39-44, 46-51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. Claims 17 & 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (Article, Model for delay faults based upon paths, 1985 International test conference, an IDS provided by the Applicant).
7. Smith substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (Page 342, Intro. Lines 1-10) testing of a clocked machine for delay failures that includes that after initial loading of the latches feeding the network, a clock is issued that causes many of these latches to take on new values, the clock that samples the output of the network into another set of latches is timed to occur at the same time interval. He thus teaches defining a fault tuple including identification of a signal line, a signal value, and a clock cycle constraint for the signal line. He does not explicitly disclose a test sequence that comprises one of more test patterns where the signal line is controlled to the signal line value during a clock cycle of the test sequence. He teaches as stated above that the clock that samples the output of the network into another set of latches is timed to occur at the same time interval after the previous clock as

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occurs during normal machine operation. It would have been obvious to a person of ordinary skill in the art to realize that he teaches a signal line that is controlled to the signal line value during a clock cycle of the test sequence, since he teaches a clock that samples the output of the network into another set of latches is timed to occur at the same time interval as the previous clock.

8. Claims 31, 38 & 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (Article, Model for delay faults based upon paths, 1985 International test conference, an IDS provided by the Applicant).

9. Smith substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (Page 342, Intro. Lines 1-10) testing of a clocked machine for delay failures that includes that after initial loading of the latches feeding the network, a clock is issued that causes many of these latches to take on new values, the clock that samples the output of the network into another set of latches is timed to occur at the same time interval. He thus teaches defining a fault tuple including identification of a signal line, a signal value, and a clock cycle constraint for the signal line. He does not explicitly disclose a test sequence that comprises one of more test patterns where the signal line is controlled to the signal line value during a clock cycle of the test sequence. He teaches as stated above that the clock that samples the output of the network another set of latches is timed to occur at the same time interval after the previous clock as occurs during normal machine operation. It would have been obvious to a person of ordinary skill in the art to realize that he teaches a signal line that is controlled to the signal line value during a clock cycle of the test sequence, since he teaches a clock that samples the output of the

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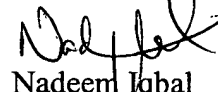
network into another set of latches is timed to occur at the same time interval as the previous clock.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (703)-308-5228. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703)-305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703)-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

  
Nadeem Iqbal  
Primary Examiner  
Art Unit 2114

NI